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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,934	10/14/2003	Hilario Oh	006601P012XD	7677

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EXAMINER

COLEMAN, WILLIAM D

ART UNIT	PAPER NUMBER
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2823

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/685,934

Applicant(s)

OH, HILARIO

Examiner

W. David Coleman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 10/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Blum et al., U.S. Patent 5,909,994.

4. Blum discloses a semiconductor process as claimed. See FIGS. 1-29, where Blum teaches the claimed limitations.

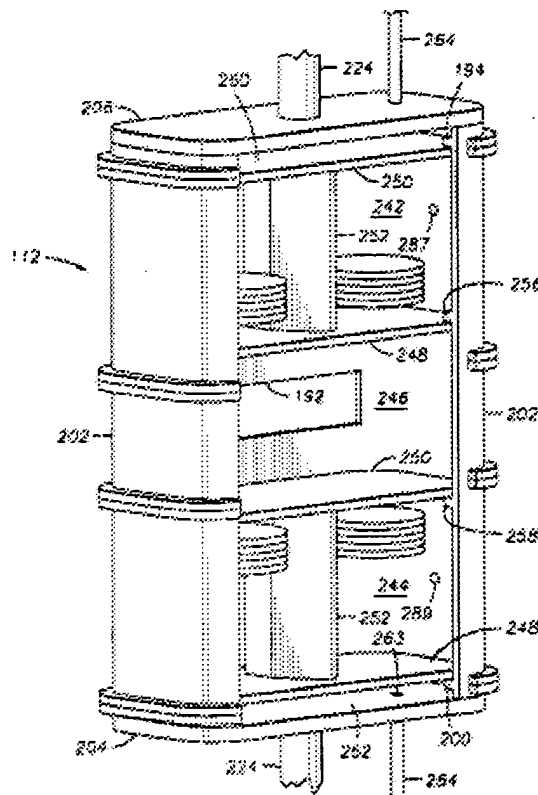
5. Pertaining to claim 1, Blum teaches a method for wafer processing comprising: loading a first plurality of wafers into a wafer cluster tool, wherein the first plurality of wafers are loaded into the cluster tool individually at intervals delimited by a first sending period, and each wafer of the first plurality of wafers is processed according to a first recipe, the first recipe including a first sequence of process steps a first plurality of process times, wherein each process

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step in the first sequence of process steps has a corresponding process time in the first plurality of process times;

loading a second plurality of wafers into a wafer cluster tool, wherein the second plurality of wafers are loaded into the cluster tool individually at intervals delimited by a second sending period, and each wafer in the second plurality of wafers is processed according to a second recipe, the second recipe including a second sequence of process steps; a second plurality of process times, wherein each process step in the second sequence of process steps has a corresponding process time in the second plurality of process times;

wherein the cluster tool has a transition period, during which the cluster tool processes one or more wafers from the first plurality of wafers according to the first recipe and one or more wafers from the second plurality of wafers according to the second recipe.

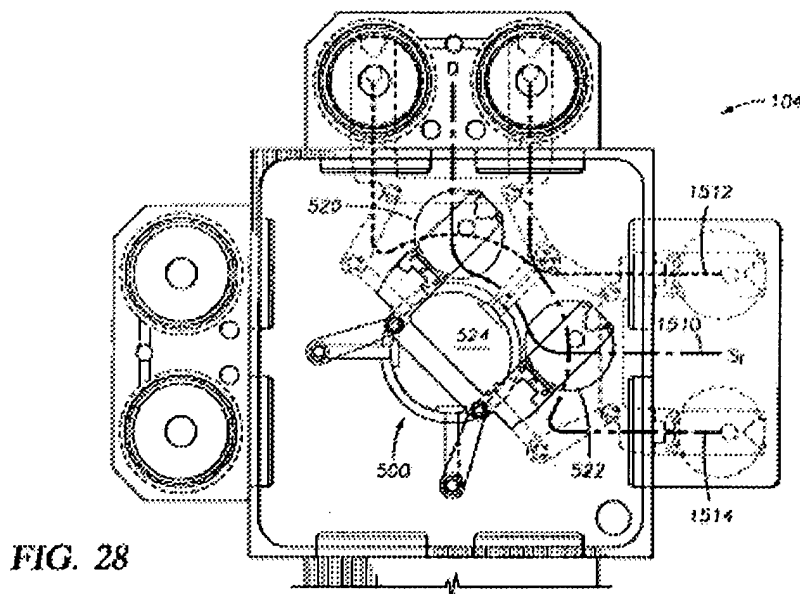


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6. Pertaining to claim 2, Blum teaches the method of claim 1, wherein the first and second sequences of process steps are identical.

Pertaining to claim 3, Blum teaches the method of claim 2, wherein the first sending period and the second sending period are equal.

7. Pertaining to claim 4, Blum teaches the method of claim 2, wherein the first and second plurality of wafers are processed in a wafer cluster tool.



8. Pertaining to claim 5, Blum teaches the method of claim 4, wherein the wafer cluster tool includes a plurality of processing chambers.

9. Pertaining to claim 6, Blum teaches the method of claim 5, wherein each process step from the first sequence of process steps is performed in a processing chamber from the plurality of processing chambers.

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10. Pertaining to claim 7, Blum teaches the method of claim 6, wherein each wafer of the first plurality of wafers is released from the wafer cluster tool at intervals delimited by the first sending period.

11. Pertaining to claim 8, Blum teaches the method of claim 7, wherein each wafer of the second plurality of wafers is released from the wafer cluster tool at intervals delimited by a second sending period.

12. Pertaining to claim 9, Blum teaches a computer program product for scheduling a wafer processing system, the computer program product comprising: (see Programming, column 20) resources for scheduling the wafer processing system during a first time period, wherein a first plurality of wafers is processed during the first time period, and each of the first plurality of wafers is processed according to a first recipe; resources for scheduling the wafer processing system during a second time period, wherein a second plurality of wafers is processed during the second time period, and each of the second plurality of wafers is processed according to a second recipe;

resources for scheduling the wafer processing system during a third time period, wherein a third plurality of wafers is processed, during the third time period, such that one or more wafers from the third plurality are processed according to the first recipe, and one or more wafers from the third plurality are processed according to the second recipe

13. Pertaining to claim 10, Blum teaches the computer program product of claim 9, wherein the computer program product resides on a server coupled to the wafer processing system.

14. Pertaining to claim 11, Blum teaches the computer program product of claim 10, wherein the wafer processing system comprises a wafer cluster tool.

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15. Pertaining to claim 12, Blum teaches the computer program product of claim 11, wherein the wafer cluster tool includes a plurality of robots for transferring the first, second, and third plurality of wafers.

16. Pertaining to claim 13, Blum teaches the computer program product of claim 12, wherein the wafer cluster tool includes a plurality of process chambers for processing the first, second, and third plurality of wafers.

17. Pertaining to claim 14, Blum teaches the computer program product of claim 13, wherein the computer program product schedules the wafer cluster tool to eliminate conflicts amongst the plurality of process chambers for use of the plurality of robots.

18. Pertaining to claim 15, Blum teaches the computer program product of claim 11, wherein the computer program product schedules the wafer processing system in real-time during the first, second, and third time periods.

19. Pertaining to claim 16, Blum teaches the computer program product of claim 10, wherein the computer program product uses a genetic algorithm to schedule the wafer processing system.

20. Pertaining to claim 17, Blum teaches the computer program product of claim 10, wherein the computer program product uses a linear transformation to schedule the wafer processing system.

21. Pertaining to claim 18, Blum teaches the computer program product of claim 10, wherein the computer program product uses a first linear transformation to schedule the wafer processing system during the first time period, uses a second linear transformation to schedule the wafer processing system during the second time period, and uses a genetic algorithm to schedule the wafer processing system during the third time period.

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22. Pertaining to claim 19, Blum teaches the computer program product of claim 10, wherein the first plurality of wafers are processed at a first constant rate.

23. Pertaining to claim 20, Blum teaches the computer program product of claim 19 wherein the second plurality of wafers are processed at a second constant rate.

24. Pertaining to claim 21, Blum teaches a method of operating a wafer cluster tool, wherein the wafer cluster tool includes a plurality of process chambers for processing a plurality of wafers, the method comprising: loading the plurality of wafers into the wafer cluster tool, wherein each wafer of the plurality of wafers is loaded after an end of one sending period, the sending period comprising a uniform time interval; processing the plurality of wafers in the cluster tool, wherein the plurality of wafers are processed concurrently in the cluster tool according to a plurality of recipes, wherein each recipe of the plurality of recipes includes a plurality of process times for the process chambers in the wafer cluster tool.

25. Pertaining to claim 22, Blum teaches the method of claim 21, wherein the plurality of wafers includes two or more wafers which are processed according to a first recipe in the plurality of recipes, and two or more wafers which are processed according to a second recipe in the plurality of recipes.

26. Pertaining to claim 23, Blum teaches the method of claim 22, wherein the wafer cluster tool includes a plurality of robots for transferring the wafers amongst the plurality of process chambers in the wafer cluster tool.

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27. Pertaining to claim 24, Blum teaches the method of claim 23, wherein a number of robots in the plurality of robots is less than a number of process chambers in the plurality of process chambers.

28. Pertaining to claim 25, Blum teaches the method of claim 24, further comprising: releasing the plurality of wafers from the wafer cluster tool, wherein each wafer of the plurality of wafers is released from the cluster tool at the end of one sending period.

29. Pertaining to claim 26, Blum teaches a method of scheduling a wafer cluster tool, wherein the wafer cluster tool is coupled to a computer system for scheduling the cluster tool, the method comprising:

inputting a plurality of recipes into the computer system, wherein each recipe of the plurality of recipes includes a plurality of process times for the cluster tool; outputting a schedule for the wafer cluster tool, such that the schedule enables the wafer cluster tool to process a plurality of wafers concurrently using the plurality of recipes, wherein each wafer of the plurality of wafers is processed at a uniform rate.

30. Pertaining to claim 27, Blum teaches the method of claim 26, wherein the schedule includes a plurality of pick-up times for a plurality of robots in the cluster tool

31. Pertaining to claim 28, Blum teaches the method of claim 2, wherein the plurality of pick-up times eliminate conflicts for the plurality of robots.

32. Pertaining to claim 29, Blum teaches the method of claim 26, wherein the schedule is computed by the computer system while the plurality of wafers is being processed.

33. Pertaining to claim 30, Blum teaches the method of claim 28, wherein a genetic algorithm is used to determine the schedule.

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34. Pertaining to claim 31, Blum teaches the method of claim 28, wherein a linear transformation is used to determine the schedule.

35. Pertaining to claim 32, Blum teaches the method of claim 28, wherein a linear transformation and a genetic algorithm are used to determine the schedule.

36. Pertaining to claim 33, Blum teaches a wafer cluster tool comprising:
a plurality of processing chambers for processing a plurality of wafers, wherein the plurality of wafers are processed according to a plurality of recipes, such that each recipe of the plurality of recipes specifies a plurality of process times for a wafer from the plurality of wafers; a plurality of wafer transporters for transporting the plurality of wafers between the process chambers;
a scheduler coupled to the wafer cluster tool, the scheduler including a computer program running on a computer system, wherein the scheduler ensures that the cluster tool processes the plurality of wafers concurrently.

37. Pertaining to claim 34, Blum teaches the wafer cluster tool of claim 33, wherein the scheduler determines a schedule for the cluster tool by use of a genetic algorithm encoded in the computer program.

38. Pertaining to claim 35, Blum teaches the wafer cluster tool of claim 33, wherein the scheduler determines a schedule for the cluster tool by use of a linear transform encoded in the computer program.

39. Pertaining to claim 36, Blum teaches the wafer cluster tool of claim 33, wherein the scheduler determines a schedule for the cluster tool in real-time, while the plurality of wafers are processed by the cluster tool.

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40. Pertaining to claim 37, Blum teaches the wafer cluster tool of claim 33, wherein the wafer cluster tool processes each wafer of the plurality of wafers at a uniform rate.

41. Pertaining to claim 38, Blum teaches the wafer cluster tool of claim 33, wherein at least one wafer transporter from the plurality of wafer transporters is used by two or more pairs of process chambers from the plurality of process chambers.

Conclusion

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

43. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

44. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC

